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(54) Method of fabrication of a microstructure having an inside cavity

(57) The present invention relates to a method of fabricating a microstructure having an inside cavity comprising the steps of:

- depositing a first layer or a first stack of layers in a substantially closed geometric configuration on a first substrate;
- performing an indent on the first layer or on the top layer of said first stack of layers;
- depositing a second layer or a second stack of layers substantially with said substantially closed geometric configuration on a second substrate;
- aligning and bonding said first substrate on said second substrate such that a microstructure having a cavity is formed according to said closed geometry configuration.

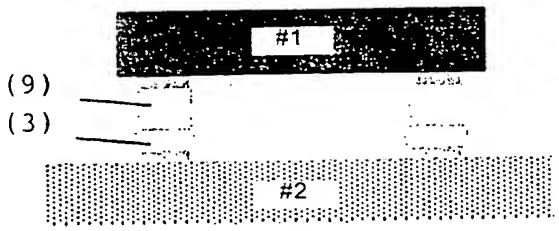

FIG. 8

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D scription

Fi ld of the invention

[0001] The present invention is related to a method of fabrication of a microstructure having an inside and preferably a sealed cavity.

[0002] The present invention is also related to the product obtained by said method, which is related to a microstructure having a sealed cavity.

[0003] The present invention is also related to specific applications of this method of fabrication of a microstructure.

Background

[0004] Microstructures having an internal cavity can be formed by making an assembly of two chips or two wafers or a chip-on-wafer with a spacer in-between. Such structures should have hermetically sealed cavities filled with a controlled ambient (gas composition and/or pressure).

[0005] These structures can be used for many different applications such as microaccelerometers, microgyroscopes, microtubes, vibration microsensors, micromirrors. micromechanical resonators or "resonant strain gauges", micromechanical filters, microswitches and microrelays.

[0006] Traditionally, for these applications, the ambient of the cavity is defined during the assembly of the several components by anodic, fusion or eutectic wafer bonding, wafer bonding using low temperature glasses or polymers as the brazing material and reactive sealing techniques.

[0007] A common drawback of these techniques is that they are rather limited in applicability, since device separation is difficult (the device has been made on one of the two wafers). It is also difficult to create electrical contacts. The drawbacks of three of the most common techniques are discussed herebelow.

[0008] The technique of diffusion bonding of a Si cap wafer on the device wafer requires flat Si surfaces and a high temperature process.

[0009] Wafer bonding techniques such as anodic bonding and silicon fusion bonding require a very clean environment, i.e., low particle contamination. There are applications that are not compatible with these boundary conditions of temperature and flatness. Furthermore, the technique of anodic bounding also requires flat surfaces and needs the application of a high voltage in order to achieve the bonding.

[0010] Finally, the technique of gluing does not provide a real hermetic bond.

[0011] US-5296408 describes a fabrication method of making a microstructure having a vacuum sealed cavity therein, including the process steps of forming an aluminum filled cavity in a body of silicon material and heating the structure such that the aluminum is absorbed into the silicon material leaving a vacuum in the cavity. In one embodiment, a cavity is etched into a silicon wafer and filled with aluminum. A silicon dioxide layer is formed over the aluminum filled cavity and the structure is heated to produce the vacuum cavity.

[0012] The document *"Fluxless flip-chip technology"* by Patrice Caillat and Gérard Nicolas of LETI, published at the First International Flip-Chip Symposium, San Jose, California, February 1994 describes a flip-chip assembly of two chips with a solder sealing ring defining a cavity during the assembly itself. The assembly and the subsequent sealing are normally done in air or under an N_2 purge. Similar conditions may exists for the other wafer bonding techniques as mentioned hereabove (except for the technique of reactive sealing).

Aims of the present invention

[0013] The present invention aims to suggest a method of fabrication of a microstructure having an inside cavity. More particularly, the present invention aims to suggest to have a sealed cavity with a controlled ambient allowing a free choice of the sealing gas composition and the sealing pressure or a vacuum.

[0014] Another aim of the present invention is to suggest a method which does not require special equipment to perform the fabrication of such microstructures in a vacuum or controlled inert gas ambient.

[0015] Another aim of the present invention is to suggest a method suited for micro-electromechanical systems (MEMS) packaging wherein all the process steps are compatible with packaging equipment.

Summary of the present invention

[0016] The present invention is related to a method of fabricating a microstructure having an inside cavity, comprising :

- making a first layer or a first stack of layers in a substantially closed geometric configuration on a first substrate;
- creating an indent on the first layer or on the top layer of said first stack of layers;
- making a second layer or a second stack of layers substantially with said substantially closed geometric configuration on a second substrate;
- aligning and bonding said first substrate to said second substrate such that a microstructure having an inside cavity is formed according to said closed geometry configuration.

[0017] The indent preferably is formed with a groove made in one of the a layers such that when the two substrates are secured together, a connection, preferably a contacting channel, between the inside cavity of a microstructure and the outside ambient is created.

[0018] Such an indent can be made using a variety of

different techniques including lithographic and/or chemical techniques or mechanical techniques removing a part of the first layer using a tool such as a shearing tool or cutting tool by applying a force using an indent tool on the first layer or by other steps.

[0019] As used herein, the term "making a layer on a substrate" means any type of method of providing a layer as the substrate including depositing or growing a layer on the substrate.

[0020] After the two substrates are secured together the indent is closed by reflowing the first layer at a reflow temperature. The reflow temperature is preferably at a temperature at which said first layer, or at least the top layer of the first stack of layers, is fusible but not the substrate and/or the other materials thereon. The reflow temperature can be lower than the melting temperature of the first layer or of one of the layers (the top layer) of the first stack of layers, the temperature being just high enough to achieve the closing of the indent and/or the corresponding fusion of the two substrates. The reflow temperature can also be equal to or above said melting temperature. Thus the reflow temperature is the temperature at which the first layer or the top layer of the first stack of layers has sufficient plasticivity to reflow for closing the indent and achieving at the same time the fusion of the two substrates.

[0021] The inside cavity can contain any kind of device with a predetermined vacuum or inert gas (N_2, He, Ar, Xe, ...) atmosphere or any other kind of gaseous atmosphere.

[0022] One of the embodiments of the present invention makes use of a solder sealing ring that can be combined with standard solder bumps for electrical contact.

[0023] Advantages of the technique of the present invention include flexible packaging of devices. A good electrical contact between device and package is also made possible, the second or the first substrate can be a more complex device by itself, a hermetic cavity sealing can be achieved and the technique can be executed to a large extent at wafer-level.

[0024] It is a further advantage of bonding techniques based on a solder bond, that are less susceptible to particles. Furthermore, flip-chip solder bonds also have the interesting property of self-alignment (within certain limits) and display a good control, predictability and reproducibility of the solder height and thus the cavity height. Furthermore, a solder bond leads to a metallic seal, which is known to provide the best hermeticity possible. Also, the metallic seal can be used as an electrical feedthrough from one chip (e.g. the bottom chip) to the other (e.g. the top chip of the stack).

[0025] Further characteristics or advantages will be found in the following description of several preferred embodiments of the present invention.

Brief description of th drawings

[0026] Figures 1 to 6 represent the several steps of a preferred embodiment of the method of fabrication of a microstructure having a sealed cavity according to the present invention.

[0027] Figures 7 and 8 represent the two last steps of a second preferred embodiment of fabrication of a microstructure having a sealed cavity according to the present invention.

[0028] Figures 9 to 11 respectively represent in detail three alternative embodiments of methods of creating the indent in the fabrication of a microstructure having a sealed cavity according to the present invention.

[0029] Figures 12 to 15 respectively represent several examples of applications of microstructures fabricated according to the method of the present invention.

[0030] Figure 16 represents a schematic cross section of a micro-relay in a package made in accordance with the principles of the present invention.

[0031] Figure 17 represents the process-flow in order to fabricate the electromagnet chip which is the bottom chip of Fig. 16. starting from a FeSi substrate.

[0032] Figure 18 represents the process-flow of the fabrication of the armature chip which is the upper chip of Fig. 16 starting from a silicon substrate.

Detailed description of preferred embodiments of the present invention

[0033] The present invention will be described more in detail hereunder referring to specific embodiments which are more precisely described in the drawings.

[0034] The method of fabrication of a microstructure having a sealed cavity, according to the present invention can be referred to as the indent-reflow-sealing (IRS) technique, which is based on a flip-chip technique using a fluxless soldering process, and which allows one to make hermetically sealed cavities with a controlled ambient (gas (es) and pressure) preferably at low temperature (typically of the order of 300 °C).

[0035] By controlled ambient, it should be understood that the inside ambient in the cavity is not in direct contact with the outside ambient. The pressure (or vacuum) in the cavity and/or its gas composition can therefore be adapted to the user requirements. The pressured (or vacuum) atmosphere in the cavity and/or its gas composition also can be adapted while forming the cavity.

[0036] The cavities are preferably formed by making an assembly of two chips (or two wafers, or chip-on-wafer) with a spacer in between. The spacer typically consists of a solder layer with or without an additional spacer layer. The alignment is done as a pick-&-place operation (in particular applicable for chip-on-wafer processes) on a flip-chip aligner/bonder. One of the advantages of the present invention is that the sealing is done in an oven as a post-assembly operation, i.e., not during the assembly operation itself. The fact that the cavity sealing is done in an oven makes the present method more flexible with respect to the choice of the sealing gas and the sealing pressure. Standard flip-chip assembly as

used by Caillat et al. in the prior art, is done in air ambient, with or without a nitrogen flow over the devices.

[0037] From a manufacturing standpoint, it should further be noted that the IRS technique according to the present invention has a cost advantage as compared to the other methods of the state of the art. The pick-&-place operation done on the flip-chip aligner-&-bonder is in general the most time-consuming and most expensive step. By doing the reflow operating as a post-assembly step in an oven, the operate time on the flip-chip aligner is (drastically) reduced. In addition, large batches of chip-on-wafer (or chip-on-chip) assemblies can be sealed in an oven at the same time. All this results in a high throughput and reduction in manufacturing costs.

[0038] An element of the method according to the present invention is that the solder reflow and sealing is done in an oven as a post-assembly operation, not during the flip-chip assembly operation itself. This makes the present technique more flexible with respect to the choice of the sealing gas and the sealing pressure as compared to the prior art method used by Caillat et al. Furthermore, from a manufacturing standpoint it is concluded that a cost advantage is expected for the present technique. The pick & place operation done in the flip-chip aligner & bonder is in general the most time-consuming and most expensive step. By doing the reflow operation as a post-assembly step in an oven, the operate time on the flip-chip aligner is (drastically) reduced. In addition, large batches of chip-on-wafer (or chip-on-chip) assemblies can be sealed in an oven simultaneously. This will result in a higher throughput and reduction in manufacturing cost.

[0039] A specific embodiment of the method of fabrication of a microstructure according to the present invention, which is based on the assembly chip-on-chip will be described hereunder with reference to the figures 1 to 6, wherein an explanation of the different processing steps follows hereunder:

[0040] **Step 1:** Preparation of the first chip (figure 1)

- deposition and patterning of a metallization seed layer (5) on the first substrate or on a first chip (1),
- preparation of a plating mould (e.g., polyimide which can be as thick as 100 μm) and electrodeposition (electroplating) of the solder (3). Some examples of possible solders can be SnPb63/37, SnPb5/95, SnPbAg (2% Ag), In, AuSn (80/20), SnAg, SnAgCu or SnBi,
- removing the mould and making the indent or groove (4). This can also be conveniently done on wafer level, the wafer is next diced to obtain the individual chips.

[0041] Advantages of using solder in the method of the present invention are as follows:

- the solder is of a soft material, thus allowing an indent to be made using a shearing tool or an indenting tool (soft should be understood as opposed to brittle, hard). The indent can be made in a photolithographic and/or chemical manner, or through mechanical means.
- the solder can be reflowed at moderate temperatures (200-350 °C) well below the melting point of the substrate. Due to the high surface tension, the indent will completely disappear after reflow (the solder is brought back into its shape without any traces of the indent):
- the solder can be electroplated using LIGA-like processing. It is thus convenient to define a geometrically enclosed structure forming an inside sealed cavity afterwards. In addition, electrodeposition allows the fabrication of high cavity walls (> 5 μm). This facilitates the making of the indent as well.
- the solder leads to an excellent hermetic seal of the cavity.

[0042] **Step 2 :** Preparation of the second substrate or chip (figure 2)

- deposition and patterning of a suitable metallization layer (6) on the second chip (2) (this can also be conveniently done on wafer level). The requirements for a suitable metallization layer should be adequately wettable and form a stable intermetallic compound with solder (3). For instance, if a SnPb-base solder is used in Step 1, most stable SnCu will be convenient. A seed layer of SnNi can also be used. Therefore, the SnNi layer needs also to be covered by a thin Au layer since Ni oxidises in air. A thickness of the Au layer will be in the range of 0.1 - 0.3 μm in order to be adequately wettable, while having a thicker Au layer will result in an unreliable solder connection. If a AuSn-base solder is used, a Au metallization will yield good results. This metallization will serve as the counter metallization for the flip-chip operation (see step 3).

[0043] **Step 3 :** Pre-treatment "flip-chip" alignment (figure 3)

- On a flip-chip aligner & bonding device, both chips (1 & 2) are aligned so that the solder ring (3) on the first chip (1) is aligned with the metal ring (6) on the second chip (2) . Before loading, both chips are preferably given an adequate plasma pre-treatment in order to achieve a reliable adhesion (so-called "prebond", see step 4) of both chips without solder reflow.

[0044] **Step 4 :** Pre-bonding (figure 4)

- Both chips are heated to a temperature well below the melting point of the solder (a softening temperature that is well below the reflow temperature), for instance for SnPb (67/37) having a melting point

183 °C, the chips are typically heated to a temperature comprised between 120-160°C. The chips are next prebonded by applying a bonding force (F), (typically of 2000 gf). The chips now "stick" and can be moved to the reflow oven. The exact temperature and bonding force depend on the solder, the solder history and the type of metallization used.

[0045] **Step 5** : Pump vacuum and filling of the cavity (figure 5)

- In the reflow oven, the cavity (8) is evacuated and next filled with the desired gas such as N_2 or a gas mixture such as N_2/H_2 mixture or even SF6 to a required pressure. Optionally, the cavity could be evacuated to a vacuum pressure.

[0046] **Step 6** : Reflow and sealing (figure 6)

- The temperature of the oven is now raised to about or above the melting point of the solder but below the melting point of all other materials used. The solder (3) will melt so as to close the indent resulting in a hermetically sealed cavity with a controlled ambient.

[0047] The process flow as represented in figs. 1 to 6 shows an assembly in which the cavity height is set by the solder itself, without using any additional spacer layer. However, the method of assembling product with an additional spacer layer is described in reference to figure 7 and 8.

[0048] Figures 7 and 8 represent the last two process steps of the method of fabrication according to the present invention using a spacer layer (9) in combination with the solder layer (3) according to said cavity height.

[0049] Figures 9, 10, and 11 represent in detail three methods of creating an indent in the preparation of one of the two chips.

[0050] More particularly, figures 9 represents local electrodeposition of the solder using a patterned mould (comparable to LIGA as 3D-microforming techniques), wherein:

- figure 9a shows the deposition of a seed layer (95), the growing of a mould material (910) (e.g. photoresist, polyimide), and the patterning of the mould (910);
- figure 9b shows the electrodeposition of the solder (93);
- figure 9c shows the removing of the mould (910) and seed layer (95) (locally).

[0051] Figure 10 represents a second method of creating an indentation by removing the solder using a shearing tool such as a shear tester.

[0052] Figure 11 represents a third method of creating an indentation by using an indenter wherein the indent of the solder is made by applying a (high) force.

[0053] The two last embodiments represented in figures 10 and 11 are possible because the solder is a soft material that allows an indentation by forcing a tool such as a shearing or an indenting tool.

[0054] Figures 12 to 15 represent several structures using the method of fabrication of a microstructure having a sealed cavity according to the present invention for specific applications such as a microreed switch (figure 12), a capacitive microaccelerator (figure 13), a vacuum microtriode (figure 14), a one-port microresonator using electrostatic drive/sense (figure 15), a microrelay (not represented), pressure sensors, light mirror devices, radiation (infrared up to X-rays) sensitive devices such as micropiles and bolometers. It is an advantage of the present invention that these devices are bulk or surface micro-machines having delicate surface structures such as membranes and moving parts. Therefore, they can not be encapsulated with a plastic moulding compound.

[0055] Furthermore, in several applications, these devices require access to light or electromagnetic radiation and more particularly to IR or UV light, X-rays, etc. Examples of such radiation applications are the packaging of imaging devices such as CMOS based imagers. In such case, the first or second substrate should be transparent for the electromagnetic radiation (light) or should at least comprise a portion of the substrate (a window) that is transparent for the radiation. Thus the second or first substrate can be chosen to be a material such as Ge-wafer or a Pb halogenide material or ZnS or quartz.

[0056] For some of the above-mentioned applications, a controlled atmosphere for proper operation is required, e.g. reference gas for IR sensor, nitrogen or He for low or high thermal conductivity. In packaging, the bolometer sensor disclosed in the patent application EP-A-0867702 can be an advantageous example of the packaging technique of the present invention. This technique also provides thermal isolation of the bolometer device. The thermal isolation is achieved by creating a vacuum atmosphere in the cavity. Also the presence of a noble gas of heavier atoms (Xe, Ar, ...) will be beneficial for the performance characteristics of the bolometer device.

[0057] Furthermore, in order to achieve commercial success, all these devices preferably should be produced in high volume and at low cost. The fabrication of a fully packaged electromagnetic micro-relay is hereunder described in details as a best mode embodiment of the present invention.

Best mode embodiment

[0058] An integral design and fabrication approach incorporating all the key elements of a micro-relay, i.e., actuator, electrical contacts, housing of the electrical contacts, structural design, micro-machining fabrication

process and packaging, has resulted in the micro-relay schematically shown in Fig. 16. The heart of the micro-relay comprises two "flip-chip assembled" chips (161) using the method of the present invention described hereabove.

[0059] The assembly process is based on the eutectic (162) bonding between electroplated tin lead (SnPb) and gold (Au) layers. One of the two chips of the assembly uses a ferromagnetic substrate (161) and comprises a U-core electromagnet, consisting of a double-layer Cu coil (cross section Cu winding 6x8 μm^2, total number of turns N=127), electroplated NiFe (50/50) poles (1x0.15 mm^2), and the lower electrical contact. The upper chip (162) uses an oxidised silicon substrate. The chip accomodates an armature consisting of a keeper plate (2x1.8 mm^2) and two supporting beams (1.6x0.15 mm^2) acting as springs, composed of approximately 20 μm thick electrodeposited NiFe (80/20). The keeper and the beams are suspended 1 μm above the silicon substrate (162). The upper contacts are deposited on the keeper plate. For the current design, the contacts are 0.20x0.15 mm^2 in size and are made of Au (1.5 μm on the keeper and 0.5 μm on the electromagnet). The contacts and the armature are housed in a hermetically sealed cavity, filled with either forming gas or air. The in-plane size of the cavity is defined by a metallic sealing ring, consisting of a spacer layer of electrodeposited nickel Ni covered with SnPb. Contact gap and actuation (pole) gap differ only by the total thickness of the contacts (approximately 2 μm), and are mainly set by the thickness of the Ni spacer layer, with a small contribution from the SnPb solder layer. For the current design, the contact gap spacing is approximately 22 μm, whereby the Ni spacer is close to 20 μm.

[0060] The fabrication of the electromagnet chip (161) with the multilayer coil starts with a ferromagnetic (FeSi, 3% silicon) substrate. The process-flow is represented in Fig. 17, wherein Fig. 17a represents the substrate (161) after the fabrication of the Cu coil; Fig. 17b represents the substrate (161) after "Ni-pad" and NiFe pole growing: Fig. 17c represents the substrate (161) after lapping and polishing poles and Ni pads, next deposition of the Ni-spacer and SnPb layer for the sealing ring and the feedthrough, and finally the deposition of the contact layer.

[0061] The sealing ring includes a double layer of a Ni spacer and a SnPb (e.g., eutectic 63/37) solder layer for making the flip-chip assembly bond. The fabrication process is based on 3D microforming technologies involving key steps such as electrodeposition of Cu for the coil windings and interconnects, of NiFe for the poles, of Ni for the spacer and moreover, of the SnPb solder for making the flip-chip assembly bond. Further steps are the preparation of a plating mould using BCB's (cyclotene) and lapping and polishing of the "overplated" metals. The armature chip (chip (162) in Fig. 16) uses a silicon substrate as the starting material. The process-flow is represented in Fig. 18, wherein Fig. 18a represents the substrate after patterning of the Al sacrificial layer: Fig. 18b represents the substrate after electrodeposition of the NiFe for the armature, followed by the deposition and patterning of the contact layer: and Fig. 18c represents the substrate after sacrificial layer etching of the Al in KOH.

[0062] Packaging focuses on low-cost, miniature packaging techniques. In addition to the four primary purposes of the package for integrated circuits, i.e., power distribution, signal distribution, power dissipation and mechanical support and protection, a fifth and very relevant function is to be added for micro-relays: definition of the housing and control of the ambient for the electrical contacts. The latter is referred to as 0-level packaging, as opposed to the 1-level packaging which comprises what is usually interpreted as packaging, i. e., the assembly capsule and the leads for interconnecting the assembly to the outside world.

[0063] The 0-level packaging deals with the fabrication of the cavity, which in the first place houses the electrical contacts (see Fig. 16). As such, it replaces the glass capsule of conventional reed switches and relays. The atmosphere in the capsule is generally nitrogen, forming gas or a vacuum and is tuned so as to increase the breakdown voltage and to improve the life expectancy of the switching contacts. For the micro-relay, the cavity is formed according to the low-temperature (<350 °C) flip-chip assembly process of the present invention of upper and bottom chips. The cavity is enclosed by both of these chips and by a geometrically enclosed sealing ring. For the reasons indicated before, the cavity must be hermetically sealed and must have a clean and controllable ambient. The term "Controllability" as used herein means an ambient containing a predetermined gas (e.g., nitrogen or SF_6) or gas mixture (e.g., forming gas) with a predetermined pressure (including a vacuum). As already indicated above, a metallic sealing ring can be implemented to meet the hermeticity requirements. For the under-bump-metallization (UBM), TiAu (0.02/0.12 μm) is preferably used and for the top-surface-metallization (TSM), Au is used which is simultaneously deposited with the contact layer.

[0064] Controllability of the ambient is achieved with the method of the present invention. In addition to the above requirements, an electrical feedthrough must be implemented to interconnect the electrical contacts on the armature(upper) chip to the output pads which are located on the electromagnet (bottom) chip. The metallic stack of Ni spacer and SnPb can also provide this feedthrough as shown in Fig. 16.

[0065] The size of the relay configuration of Fig. 16 is set by the bottom electromagnet chip and is approximately 5.3x4.1 mm^2. The thickness of the flip-chip assembly is approximately 1 mm.

[0066] Upon energising the coil, the keeper is attracted towards the poles, thus closing the electrical contacts. The output of the relay can either be defined by the two bottom contacts whereby the keeper merely acts

as a shorting element, or. by one (or both) bottom contacts and the upper contacts. In the latter case, the upper contact is interconnected to the output pad on the bottom chip via the supporting beams and the electrical feedthrough (Fig. 16) if a magnetic force F_m acting on the keeper is in general limited by magnetic saturation of the keeper and/or by the residual pole gap spacing after closure. For the current design, F_m is around 2 mN (saturation limited), which is calculated for a magnetomotive force NI>0.8 AT, a permeability μ_r=2,000 and a saturation induction of 1 T of the keeper material, an average keeper length of 1.6 mm and a residual gap of 1 µm. The contact force F_c (hereby assuming that pull-in has occurred) is limited by the maximum magnetic force minus the spring force, and thus, $F_c < 2$ mN/2 = 1 mN (factor 2 arises because the force is distributed over two contacts). It should be noted that the spring force is determined by the stiffness of the supporting beams but also by the stiffness of the keeper plate. The latter will deform upon closure of the contacts and this way, an additional spring stiffness is introduced.

Claims

1. A method of fabricating a microstructure having an inside cavity comprising the steps of:

   - making at least a first layer (3) in a substantially closed geometric configuration on a first substrate (1):
   - creating an indent (4) in said first layer (3);
   - making at least a second layer (6) substantially with said substantially closed geometric configuration on a second substrate (5) :
   - aligning and bonding said first substrate (1) on said second substrate (5) such that a microstructure having a cavity (8) is formed according to said closed geometry configuration.

2. A method of fabricating a microstructure having an inside cavity comprising the steps of:

   - making at least a first stack of layers in a substantially closed geometric configuration on a first substrate (1):
   - creating an indent (4) on the top layer (3) of said first stack of layers:
   - making at least a second stack of layers (6) substantially with said substantially closed geometric configuration on a second substrate (5):
   - aligning and bonding said first substrate (1) on said second substrate (5) such that a microstructure having a cavity (8) is formed according to said closed geometry configuration.

3. The method as recited in claims 1 or 2, wherein the indent is performed using photolithographic and/or chemical steps.

4. The method as recited in any one of the preceding claims, wherein the indent is performed by removing a part of said layer or at least one of the layers of the first stack of layers using a shearing tool (11).

5. The method as recited in any one of the preceding claims, wherein the indent is performed by applying a force to an indent tool (12) on said first layer or at least one of the layers of the first stack of layers.

6. The method as recited in any one of the preceding claims, wherein a pre-treatment prior to the aligning and bonding of said substrates is performed on both substrates, said pre-treatment consisting in a plasma etching treatment.

7. The method as recited in any one of the preceding claims, wherein a pre-bonding treatment is performed after the aligning of both substrates in order to form the microstructure.

8. The method as recited in any one of the preceding claims, wherein the pre-bonding treatment consists in heating the microstructure to a temperature well below the melting temperature of said first layer or at least one of the layers of the first stack of layers.

9. The method as recited in any one of the preceding claims, wherein said first layer or said first stack of layers includes a solder layer essentially made of PbSn.

10. The method as recited in any one of the preceding claims 2 to 9, wherein the first stack of layers comprises a metallization seed layer (2).

11. The method as recited in any one of the preceding claims, further comprising the step of pumping said cavity to a predetermined pressure prior to and/or while executing the bonding step.

12. The method as recited in any one of the preceding claims. further comprising the step of filling the cavity with a gas or a gas mixture to a predetermined pressure prior to and/or while executing the bonding step.

13. The method as recited in any one of the preceding claims, wherein the gas is an inert gas.

14. The method as recited any one of the preceding claims. wherein the indent is closed by reflowing the top layer of the first stack of layers at a reflow temperature above or equal to or just below the melting temperature of said first layer or at least one of the

layers of said first stack of layers.

15. The method as recited in any one of the preceding claims, wherein the reflowing is performed in a vacuum environment.

16. The method as recited in any one of the preceding claims, wherein the reflowing is performed in an inert gas environment.

17. The method as recited in any one of the preceding claims, wherein the reflowing is performed at a temperature which is less than the melting point of the substrates and the other structures thereon excluded said first layer or at least one of the layers of said first stack of layers.

18. The method as recited in any one of the preceding claims, wherein both substrates can be silicon or chips in silicon wafers or one substrate being a chip, the other substrate a wafer.

19. The method as recited in any one of the preceding claims, wherein a window is made in one of the two substrates in order to let electromagnetic radiation to enter the cavity.

20. The method as recited in any one of the preceding claims, wherein one of said substrates is transparent for electromagnetic radiation which is able to enter the cavity.

21. Microstructure having a sealed cavity (8), wherein said cavity is defined by walls according to a closed geometric configuration between two substrates (1 and 5), said walls being a stack of layers comprising at least the first metallization layer (2), a reflowed solder layer (3), and a second metallization layer (6).

22. Microstructure as recited in claim 21 wherein at least part of one of the two substrates has a window in order to let electromagnetic radiation to enter the cavity.

23. Microstructure as recited in claim 21 wherein one of said substrates is transparent for electromagnetic radiation in order to let it enter into the cavity.

24. Use of the method as recited in any one of the claims 1 to 20 for realising a microreed switch. a capacitive microaccelerator, a vacuum microtriode, a microresonator. a microrelay and a microswitch.

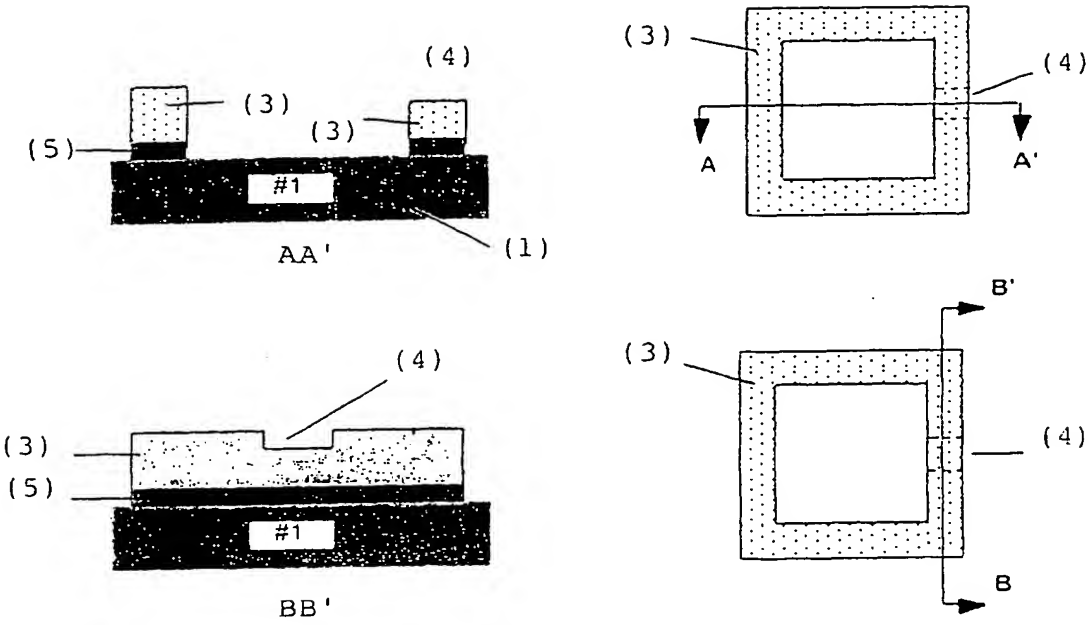


FIG. 1

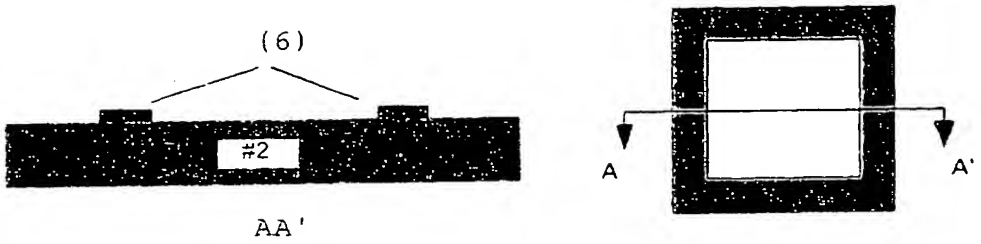


FIG. 2

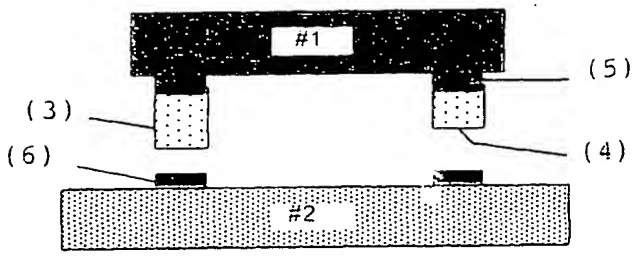
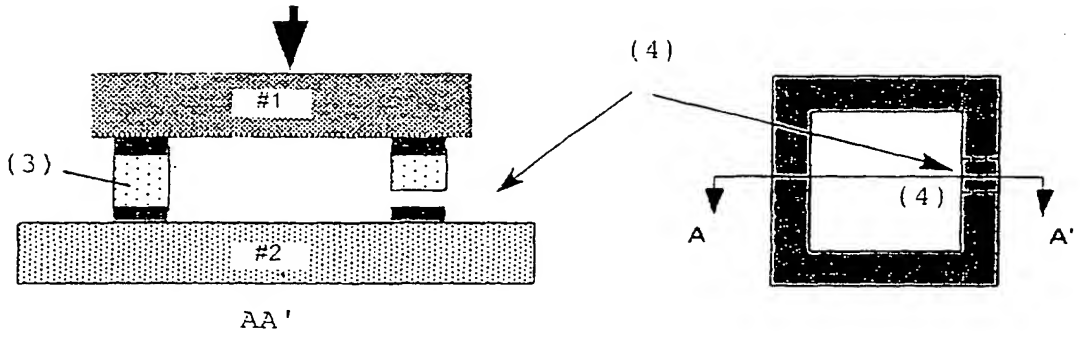


FIG. 3



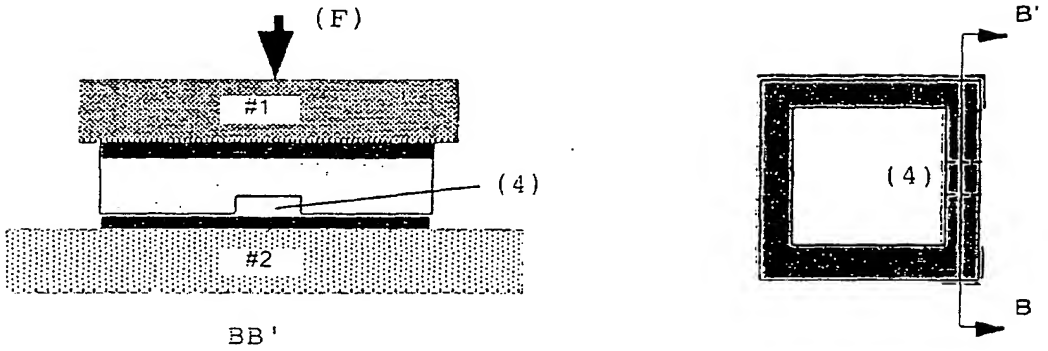


FIG. 4

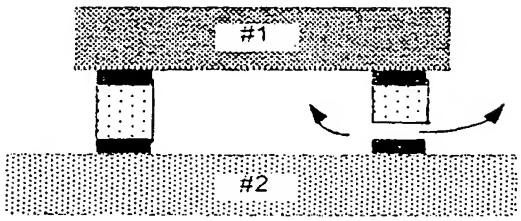


FIG. 5

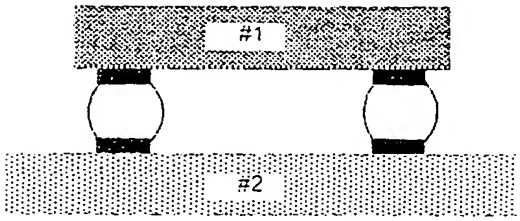


FIG. 6

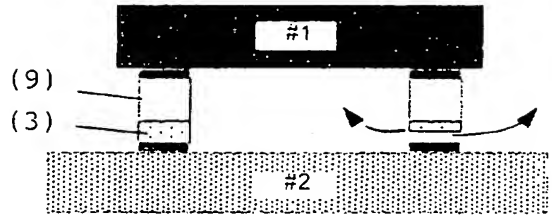


FIG. 7

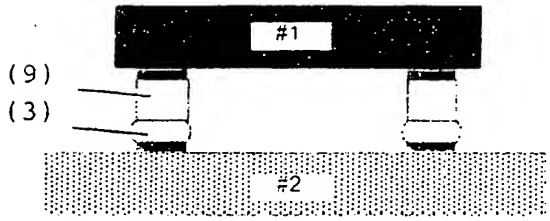


FIG. 8

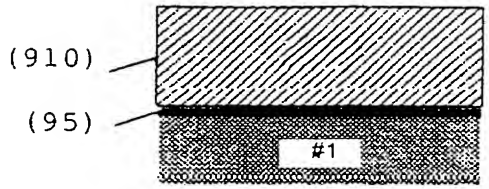


FIG. 9a

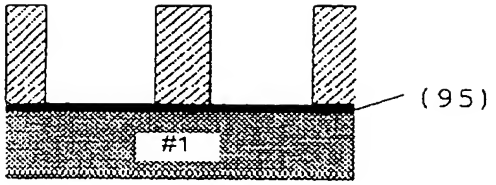


FIG. 9b

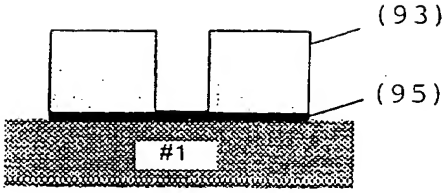


FIG. 9c

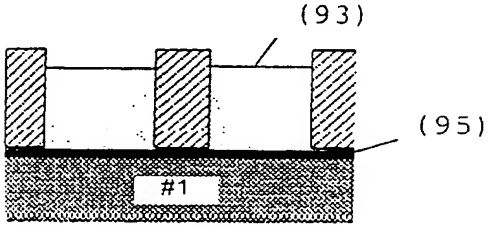
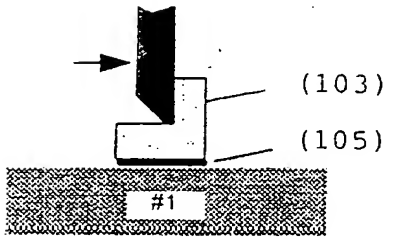


FIG. 9d



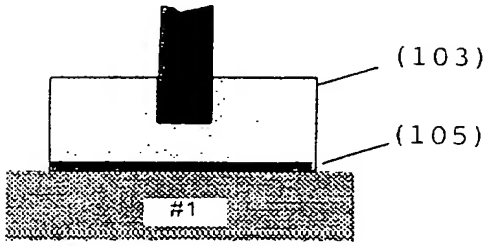
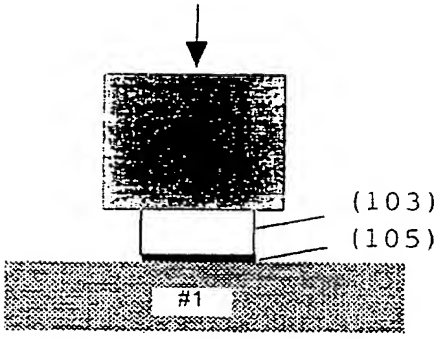


FIG. 10



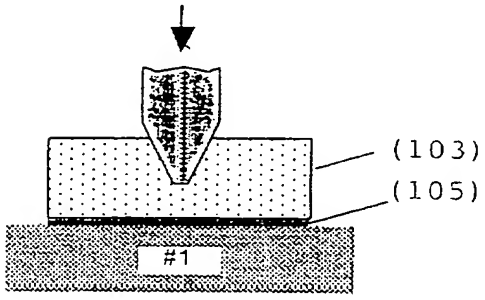


FIG. 11

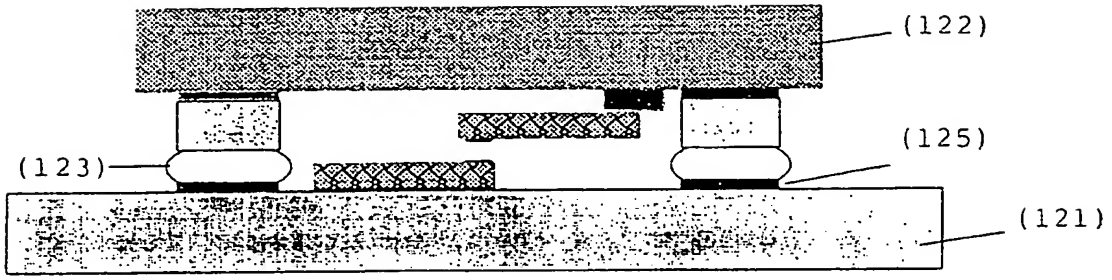


FIG. 12

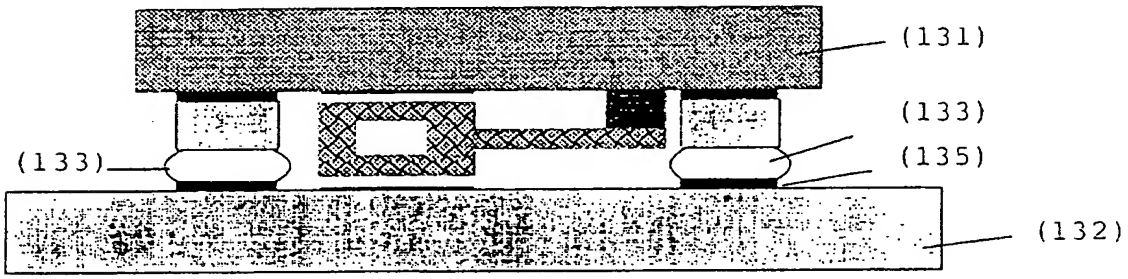


FIG. 13

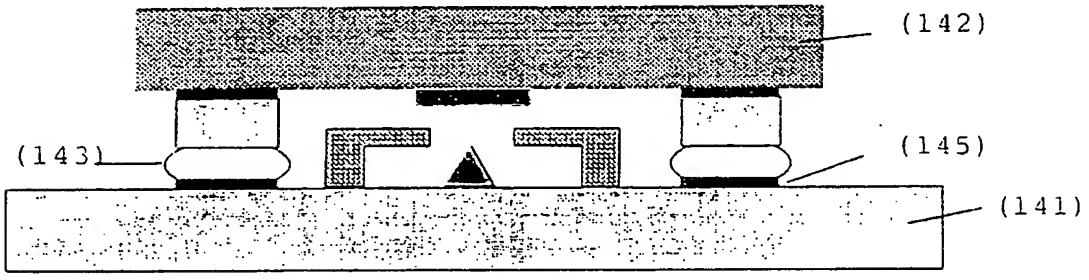


FIG. 14

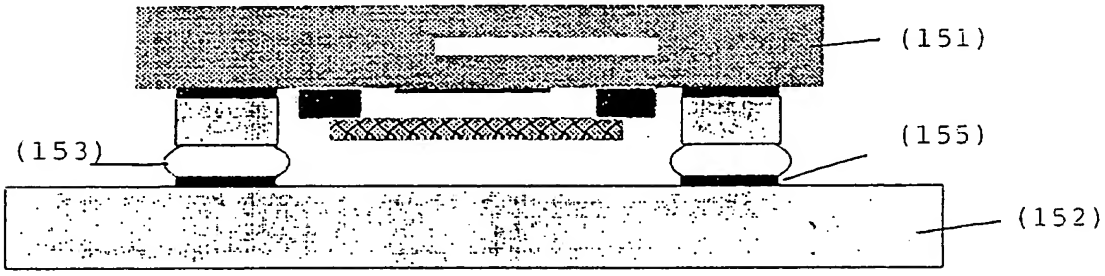


FIG. 15

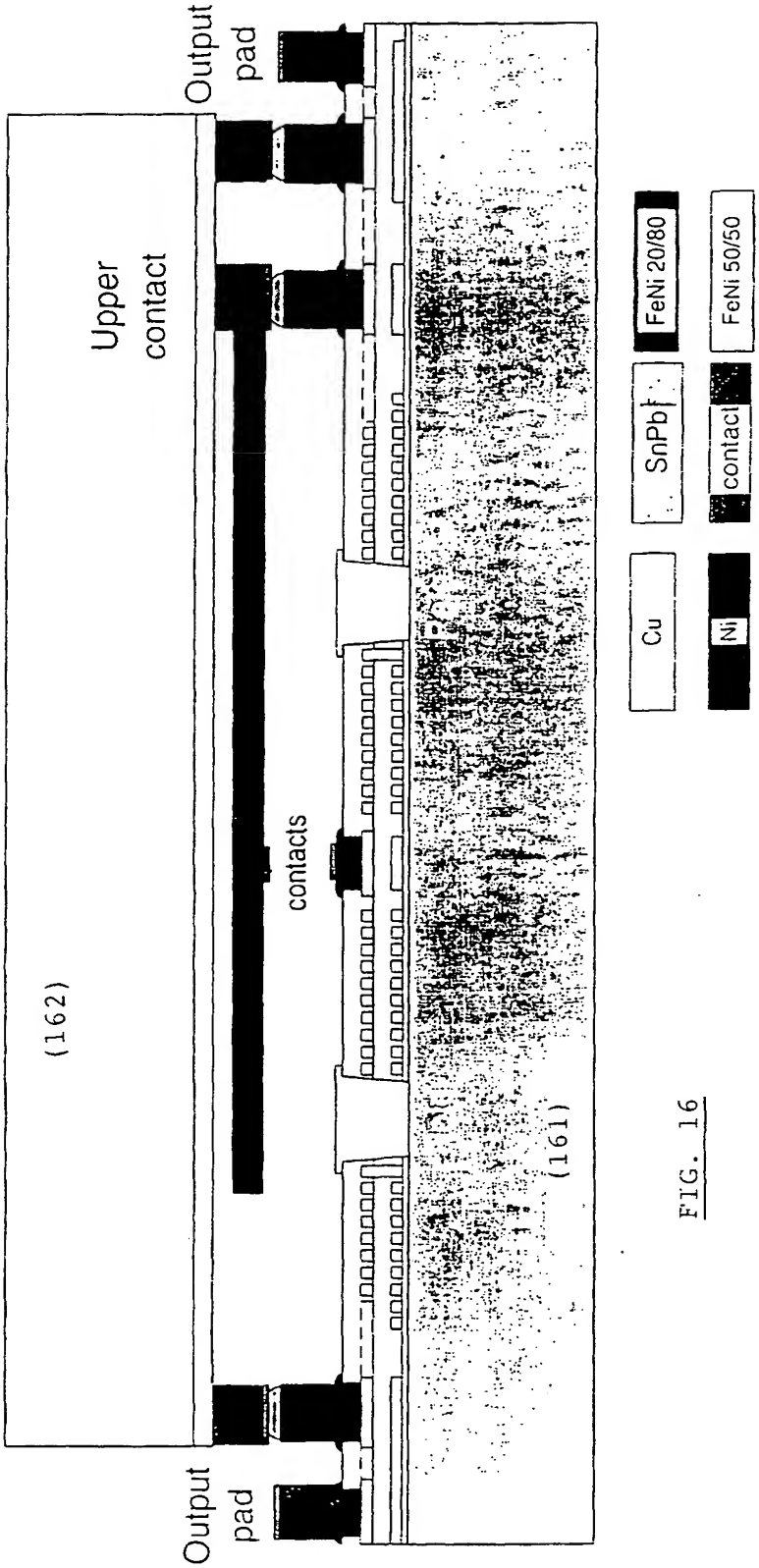

Output pad
Upper contact
(162)
contacts
(161)
Output pad
Cu
SnPb
Ni
contact
FeNi 20/80
FeNi 50/50

FIG. 16

FIG. 17

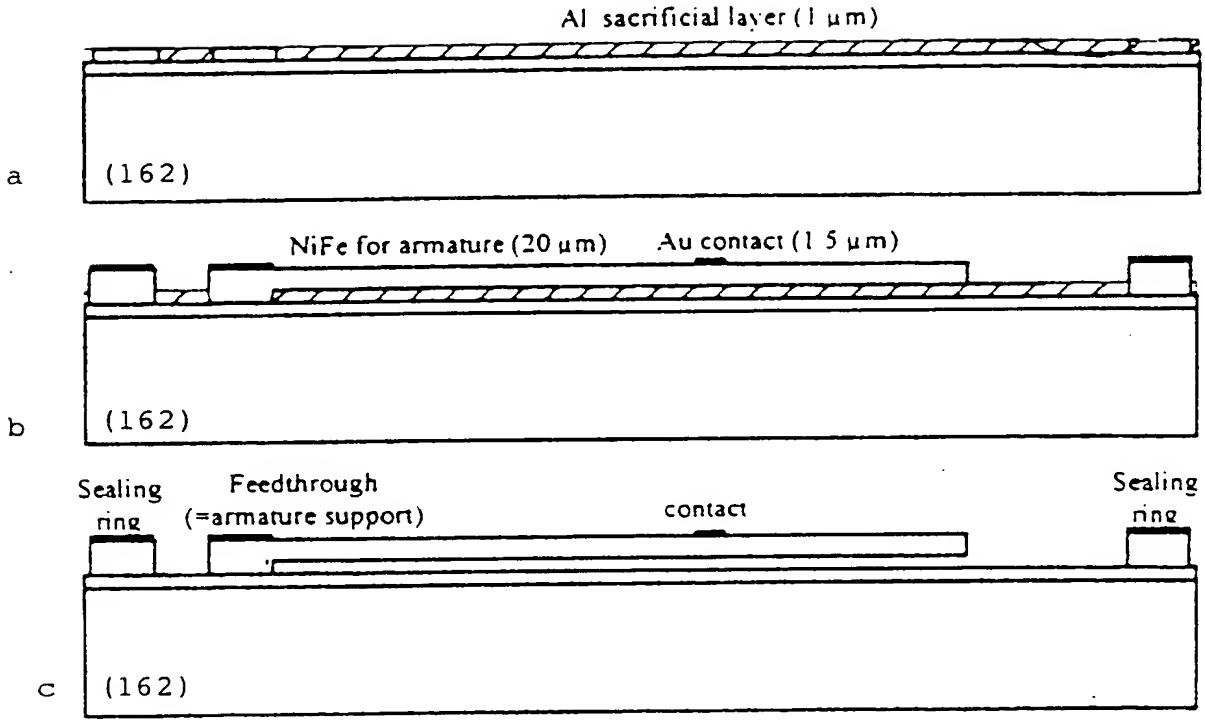
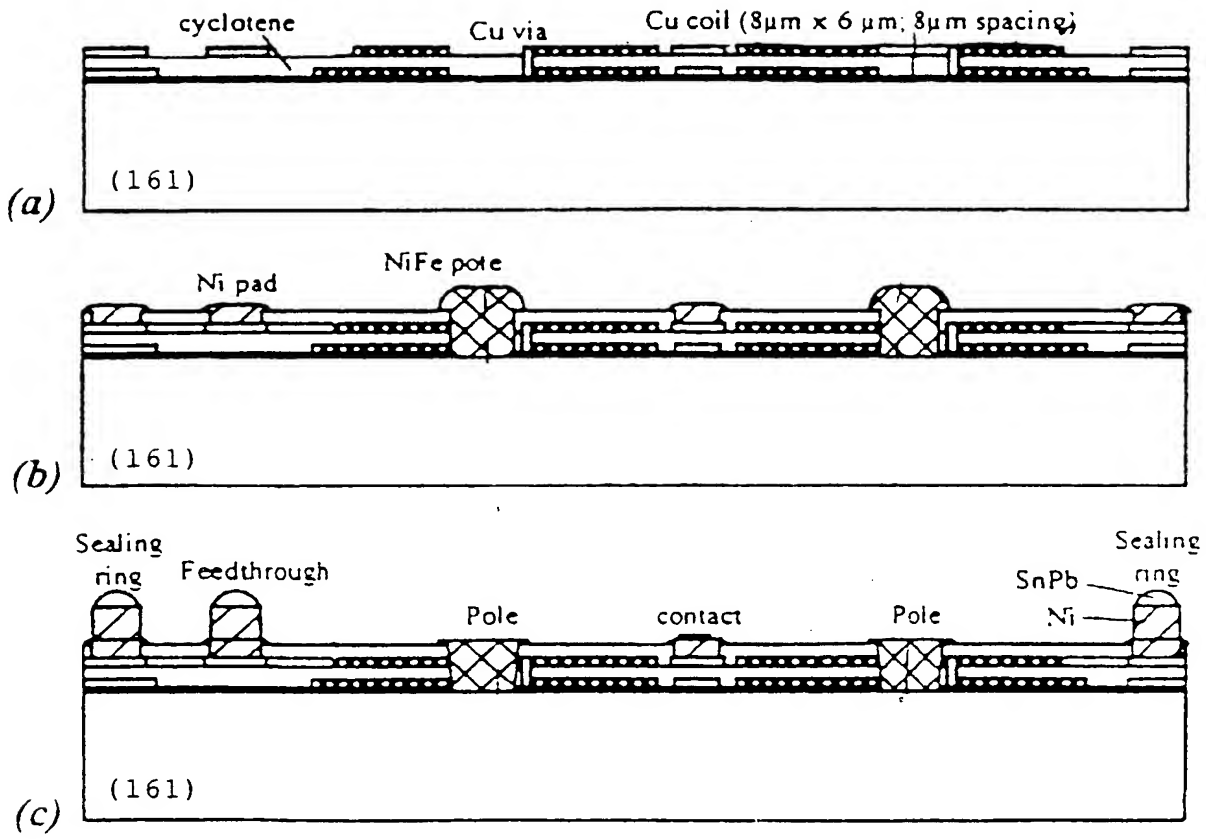

Al sacrificial layer (1 µm)
a
(162)
NiFe for armature (20 µm)
Au contact (1 5 µm)
b
(162)
Sealing ring
Feedthrough (=armature support)
contact
Sealing ring
c
(162)

FIG. 18


cyclotene
Cu via
Cu coil (8µm x 6 µm; 8µm spacing)
(161)
(a)
Ni pad
NiFe pole
(161)
(b)
Sealing ring
Feedthrough
Pole
contact
Pole
SnPb
Ni
Sealing ring
(161)
(c)

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 99 87 0071

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
P,X	EP 0 849 578 A (MURATA MANUFACTURING CO) 24 June 1998 (1998-06-24)	1,3,8, 11,12, 15,17, 18,21,24	H01L23/10 G01L9/00
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X	US 5 317 922 A (BOMBACK JOHN L ET AL) 7 June 1994 (1994-06-07)	21,24	
A	* the whole document *	1,2,5,6, 9-12,14, 15,18	
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Y		22,23	
A	* the whole document *	1,12,16, 18	
A	US 5 335 550 A (SATOU KIMITOSHI) 9 August 1994 (1994-08-09) * column 6, line 9 - column 7, line 20; figures 1-12 *	1,2,11, 15,18	
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Y	EP 0 709 659 A (VALTION TEKNILLINEN :VAISALA OY (FI)) 1 May 1996 (1996-05-01) * column 3, line 16-51; figures 1,2 *	19,22	

-/--

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H01L
G01L
B81B

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	9 August 1999	Brock, T

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L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P01C01)

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EUROPEAN SEARCH REPORT

Application Number
EP 99 87 0071

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.6)
Y	US 5 602 385 A (MATHIEU LYDIE ET AL) 11 February 1997 (1997-02-11) * the whole document *	20,23	

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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	9 August 1999	Brock, T

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